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10EC45

Fourth Semester B.E. Degree Examination, June/July 2015
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – A

1 a. Name the different types of operations in HDL. Explain the bitwise, unary and Boolean logical operations present in verilog with example. **(08 Marks)**

b. Name the VHDL data types. Explain the physical data type and composite data type in VHDL. **(06 Marks)**

c. Write the result of the following operation if A = 10010011 and B = 01101111:
i) A sr*l* 04 ii) B sla 03 iii) A << 02 iv) A % 2 v) ! (&B) vi) A & B in VHDL. **(06 Marks)**

2 a. Write the VHDL code for 2 × 2 unsigned combinational array multiplier using dataflow description. **(06 Marks)**

b. Write the verilog description for 4 bit ripple carry adder. Assume 5ns delay for all the gates and description using dataflow. **(08 Marks)**

c. Explain how signal declaration is done in VHDL and verilog. **(06 Marks)**

3 a. With the help of booth algorithm multiply the numbers (-8) × (7). Also write the VHDL code to realize the same. **(10 Marks)**

b. Write an HDL code to realize the positive edge triggered JK flip flop.
i) Use if statement in VHDL.
ii) Use case statement in verilog HDL. **(10 Marks)**

4 a. Write the logic circuit for performing 3 bit comparision using 3 full adder. Also write the structural description to realize the same in VHDL. **(10 Marks)**

b. What is binding? Explain how binding between entity and architecture is done in VHDL and also binding between library and module in VHDL. **(05 Marks)**

c. Write the truth table of a logic system having 3 input and when the odd number of inputs are high then the output of the system will be high. Also write the verilog code to realize the same using structural description. **(05 Marks)**

PART – B

5 a. What is the need of procedure and task? Explain the declaration and body of the task. **(04 Marks)**

b. Write the procedure for converting an unsigned binary to an integer. **(08 Marks)**

c. What is a function? Write the code for finding greater of two signed numbers in verilog using function. **(08 Marks)**

6 a. What is the need for mixed types description? **(04 Marks)**

b. Using package declaration declare one dimensional array type with N of elements and L number of bits in each element. Write a VHDL code for finding the largest element present in one dimensional array declared using package. **(08 Marks)**

c. Write the truth table for the SRAM shown in Fig.Q.6(c). Write a verilog HDL code to read or write the data from SRAM. **(08 Marks)**

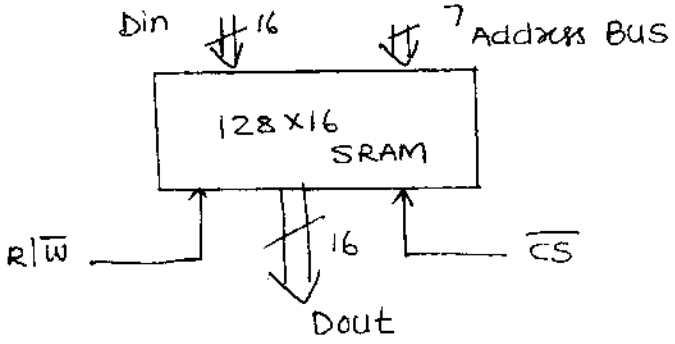

Fig.Q.6(c)

7 a. Write the mixed language description of an adder shown in Fig.Q.7(a). Invoke a VHDL full adder from verilog. **(10 Marks)**

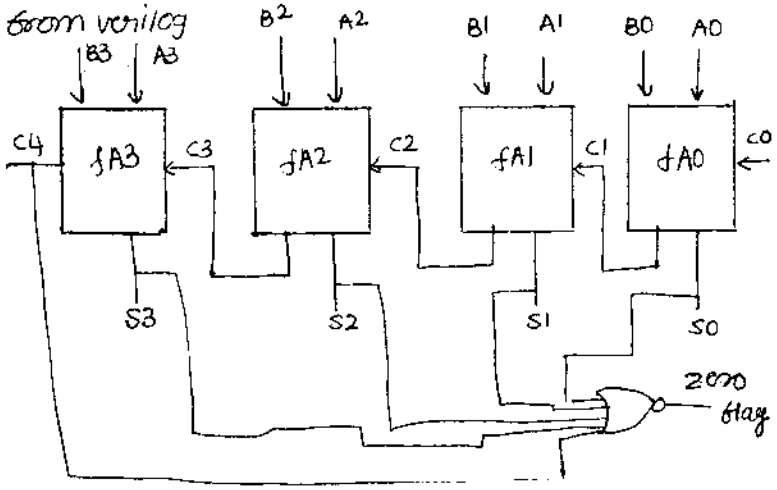

Fig.Q.7(a)

b. Write the truth table of JK flipflop with clear. Describe the JK flipflop with clear using mixed language description. **(10 Marks)**

8 a. Write the general steps of synthesis in form of a flowchart and explain it. **(10 Marks)**

b. Write VHDL and verilog code for signal assignment statement $y = 3x$ with x as of size 2 bits. Also show the mapping of this signal assignment to gate level. **(10 Marks)**

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